Description

40V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

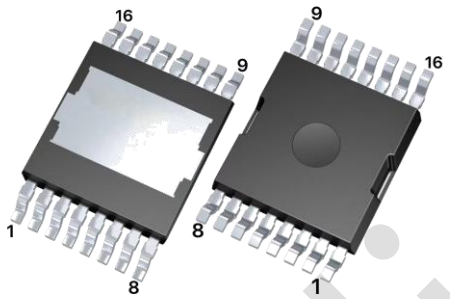
Features

- Device Rating V_{DS} = 40V, I_D = 841A
- $R_{DS(ON)}$ =0.37mΩ (typ.) @ V_{GS} = 10V, I_D = 100A
- Advanced Split Gate Trench Device Design
- RoHS Compliant & Halogen-Free
- Qualified according to JEDEC for target applications
- 100% Avalanche Test

Application

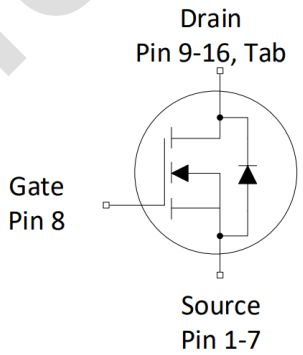
- High frequency synchronous rectifiers
- Brushless DC motor control
- Battery protection
- High performance DC/DC converters
- OR-ing and redundant power switches

Package



TOLT

JFGR45N40R



Absolute Maximum Ratings T_J=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		40	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	841	A
		T_C = 100℃	532	A
I_{DM}	Pulsed Drain Current note2		2524	A
P_D	Power Dissipation note4	T_C = 25℃	500	W
	Power Dissipation	T_A = 25℃	3.12	W
E_{AS}	Single Pulsed Avalanche Energy note3		2507	mJ
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Thermal characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1	-	0.25	-	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	40	℃/W

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Electrical Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Units
Off Characteristic							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		40	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} =40V, V_{GS}= 0V, T_C = 25℃		-	-	1	μA
		V_{DS} =40V,V_{GS} = 0V, T_C = 125℃		-	-	100	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V		-100	-	100	nA
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		1	-	2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =100A		-	0.37	0.45	mΩ
		V_{GS} = 4.5V, I_D =50A			0.41	0.50	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 1V, I_D =100A		-	570	-	S
Dynamic Characteristics							
R_g	Gate Resistance	f=1.0MHz		-	1.3	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1.0MHz		-	20577	-	pF
C_{oss}	Output Capacitance			-	4860	-	pF
C_{rss}	Reverse Transfer Capacitance			-	164	-	pF
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 100A,V_{GS} = 4.5V		-	137	-	nC
Q_g	Total Gate Charge	V_{DS} =20V, I_D = 100A, V_{GS} = 10V		-	291	-	nC
Q_{gs}	Gate-Source Charge			-	54	-	nC
Q_{gd}	Gate-Drain("Miller") Charge			-	35	-	nC
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20V, I_D = 30A, R_G = 1Ω, V_{GS} = 4.5V		-	47	-	ns
t_r	Turn-On Rise Time			-	80	-	ns
$t_{d(off)}$	Turn-Off Delay Time			-	71	-	ns
t_f	Turn-Off Fall Time			-	24	-	ns
Source-Drain Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Diode Forward Current note1,5			-	-	416	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5			-	-	2524	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 100A, V_{GS} = 0V di/dt = 100A/μs		-	124	-	ns
Q_{rr}	Reverse Recovery Charge			-	145	-	nC
V_{SD} note2	Diode Forward Voltage	I_S = 50A V_{GS} = 0V	T_J = 25°C	-	0.77	-	V
			T_J =125°C	-	0.62	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.5mH, I_{AS}= 116A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

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Typical Performance Characteristics

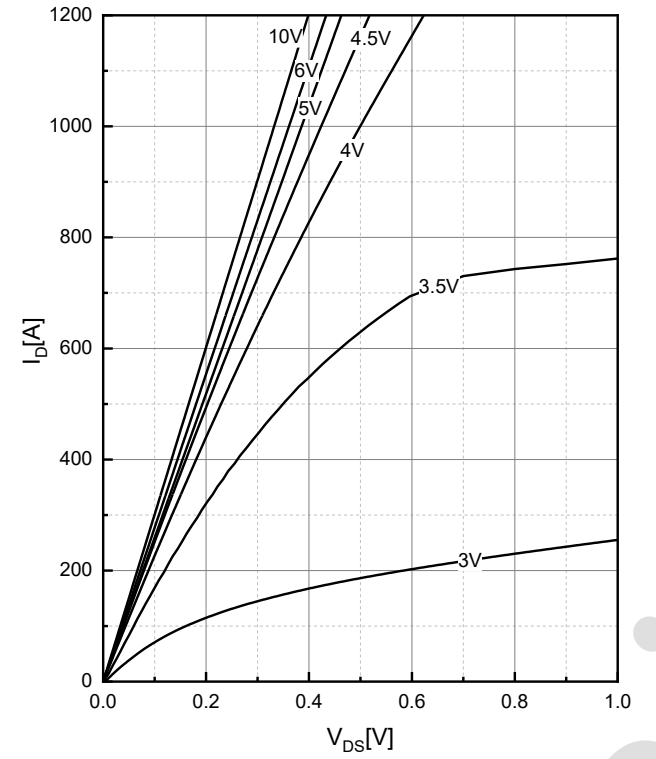

Figure 1. Output Characteristics, T_J=25℃

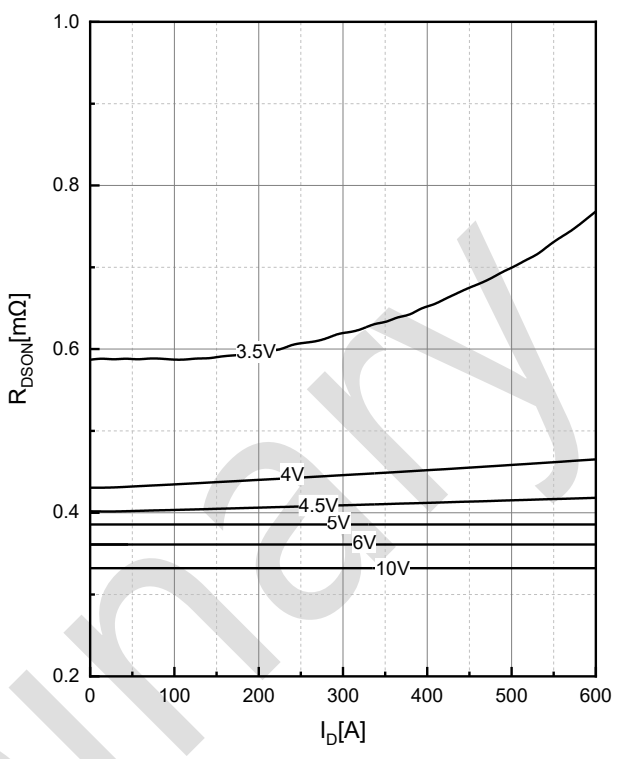

Figure 2. Drain-source on resistance , T_J=25℃

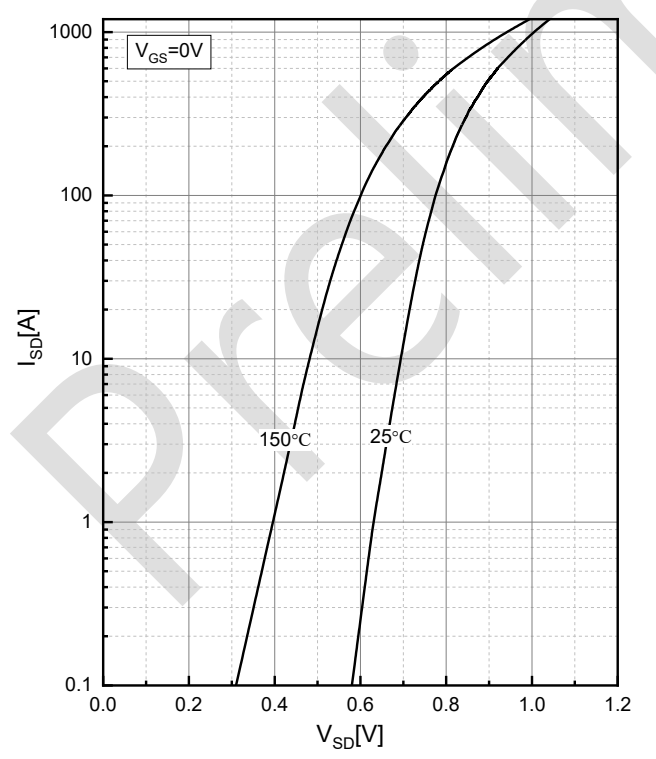

Figure 3. Forward characteristics of body diode

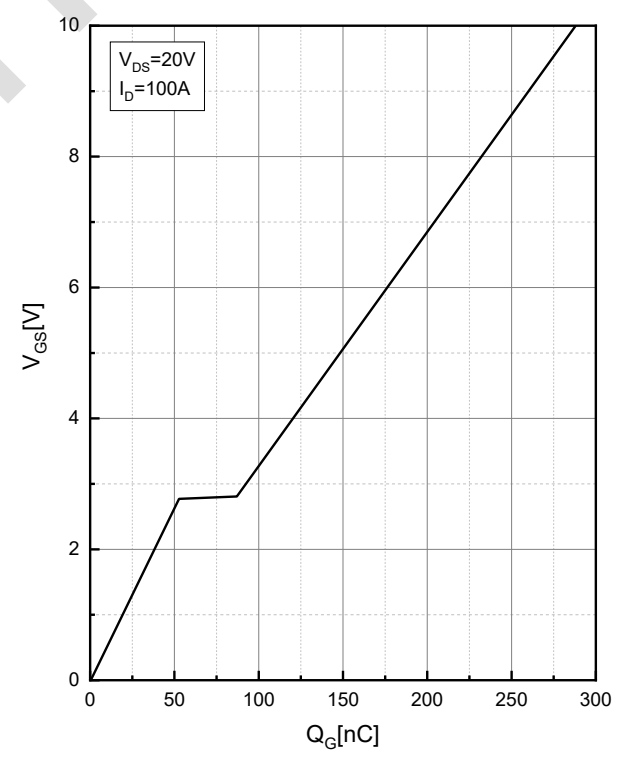

Figure 4. Gate Charge Characteristics

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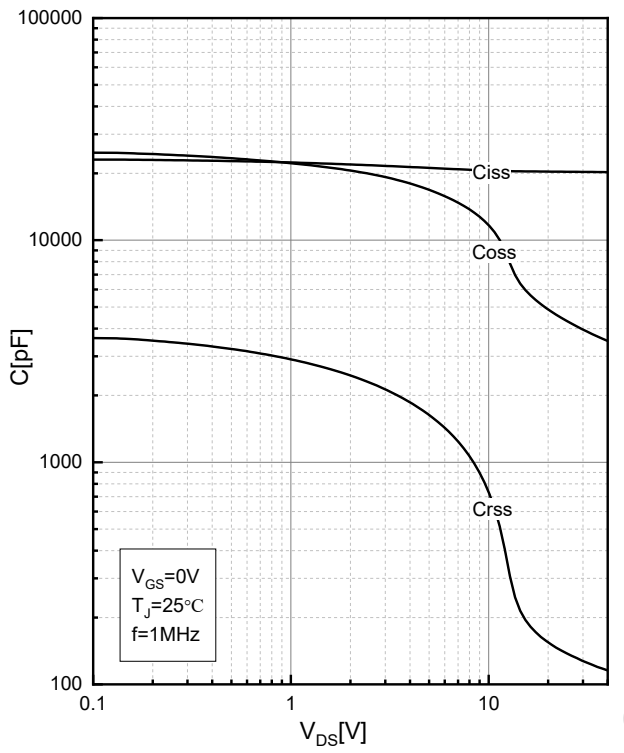

Figure 5. Capacitance Characteristics

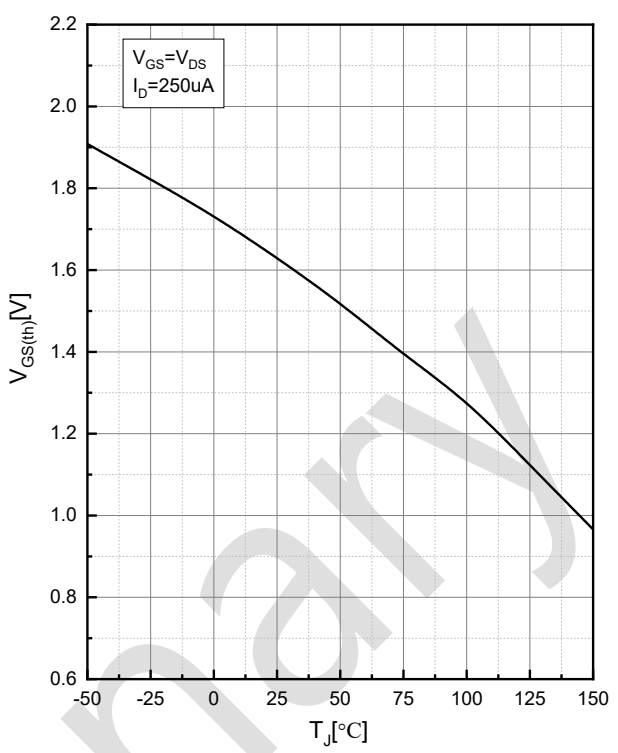

Figure 6. Threshold Voltage Vs. Temperature

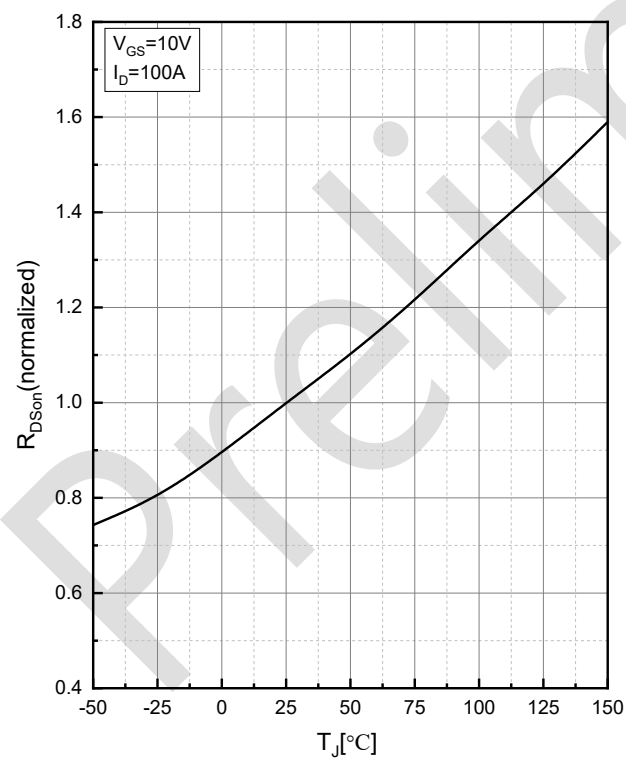

Figure 7. Drain-source on-state resistance

Figure 8. Maximum Safe Operating Area

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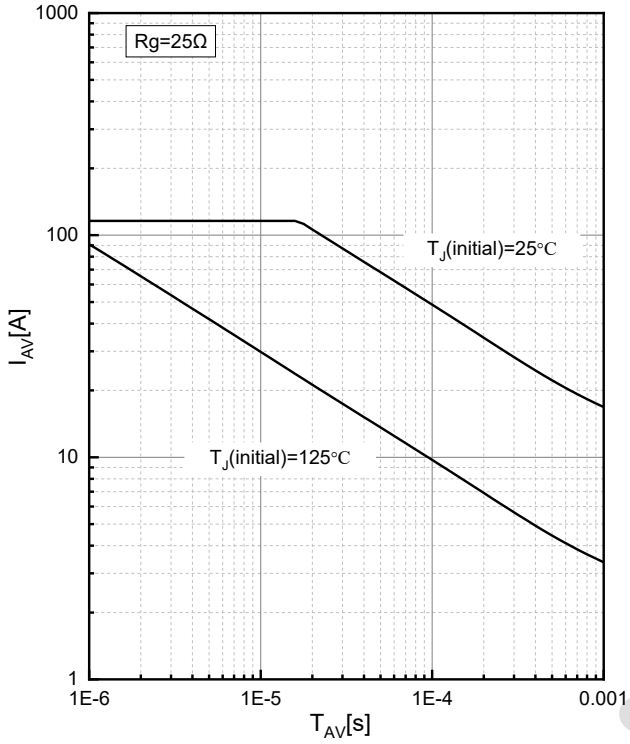

Figure 9. Avalanche characteristics

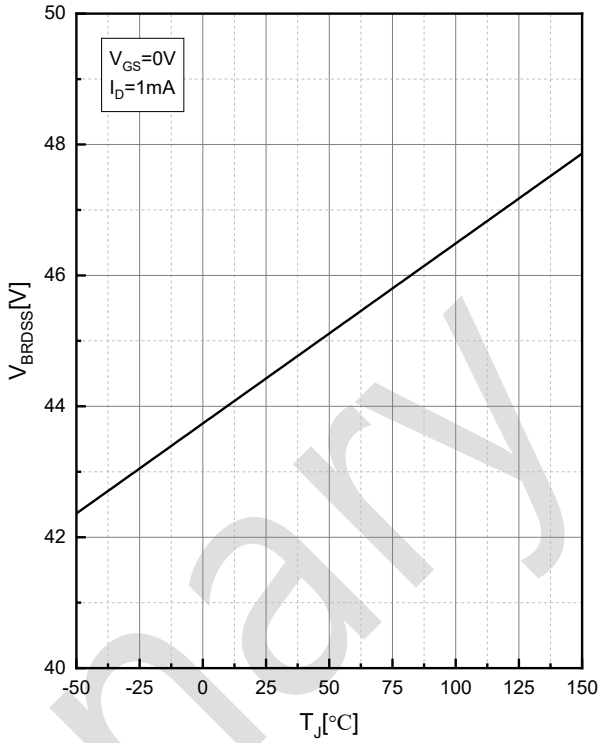

Figure 10. Drain-source breakdown voltage

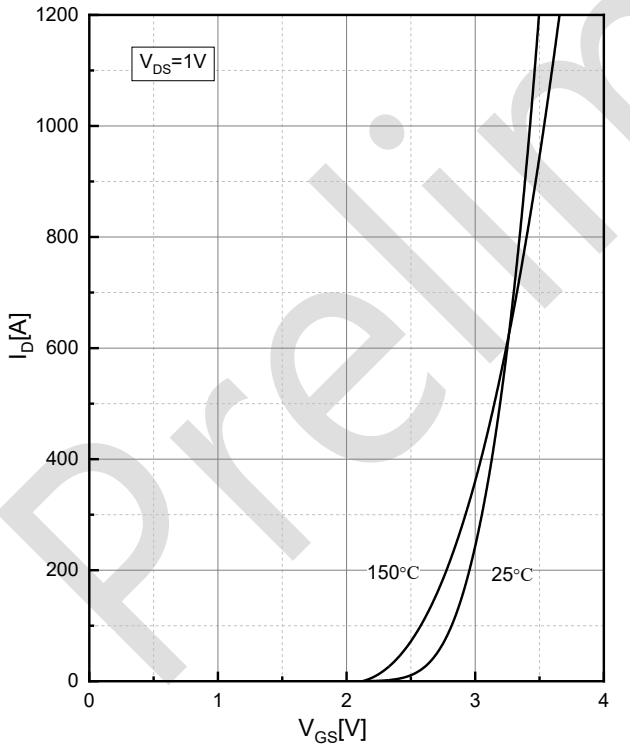

Figure 11. Transfer characteristics

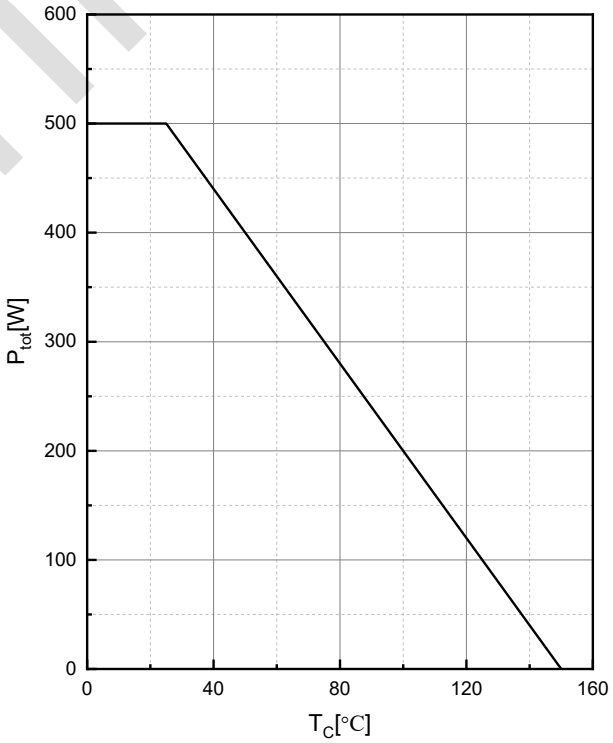

Figure 12. Power dissipation

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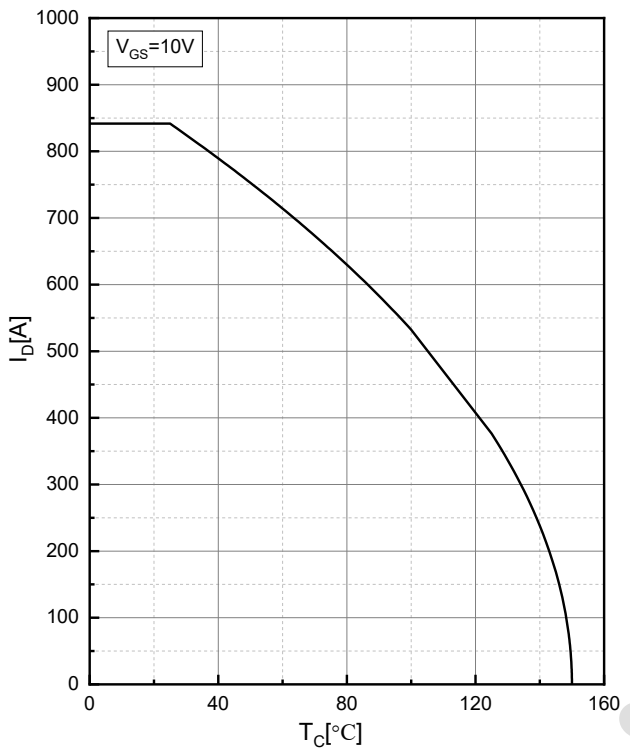

Figure 13. Drain current

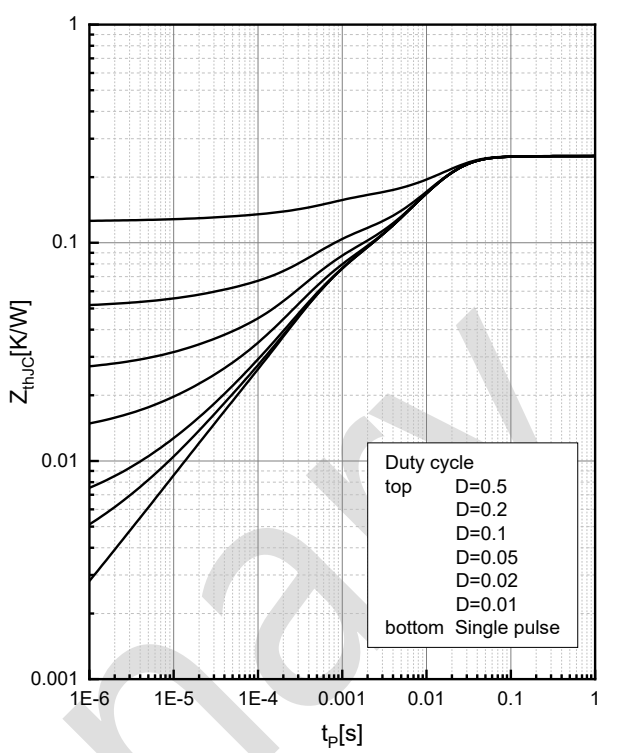

Figure 14. Effective Transient Thermal Impedance

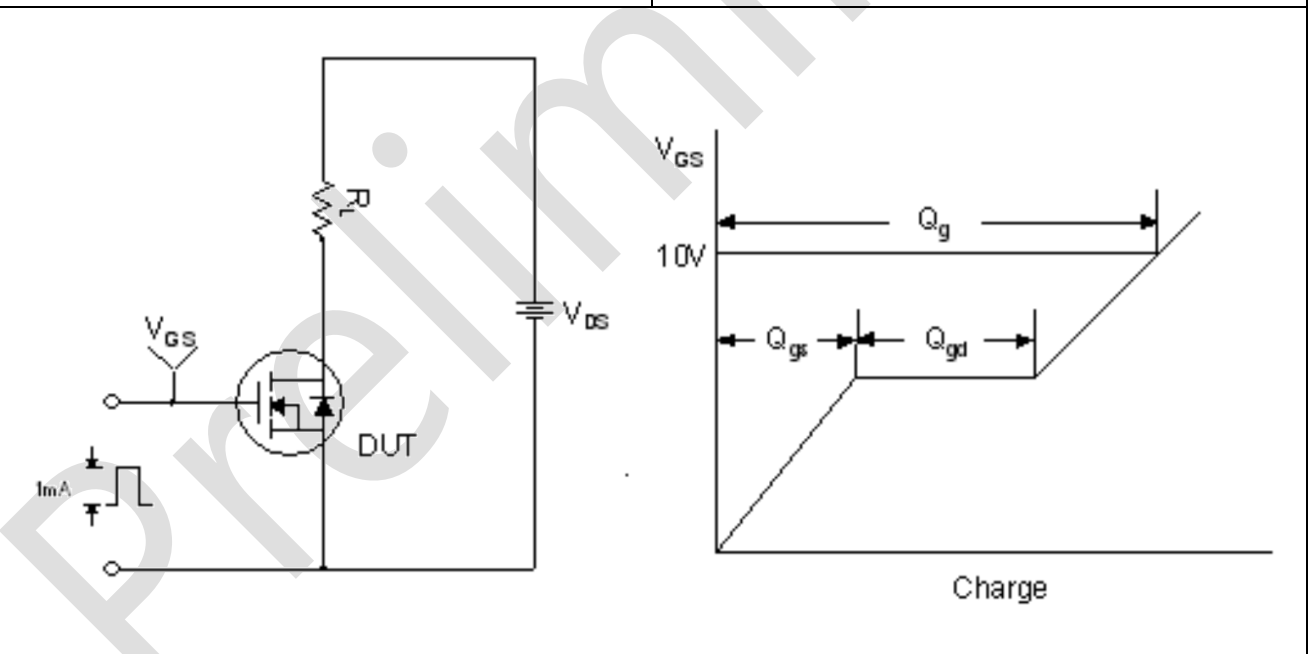

Figure 15. Gate Charge Test Circuit & Waveform

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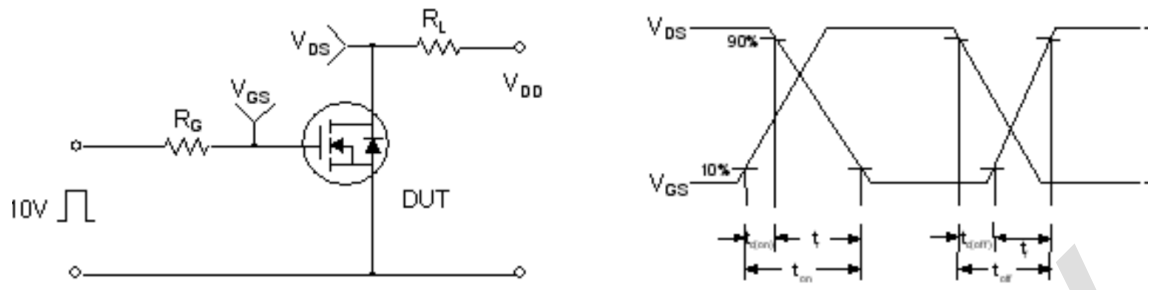

Figure 16. Resistive Switching Test Circuit & Waveforms

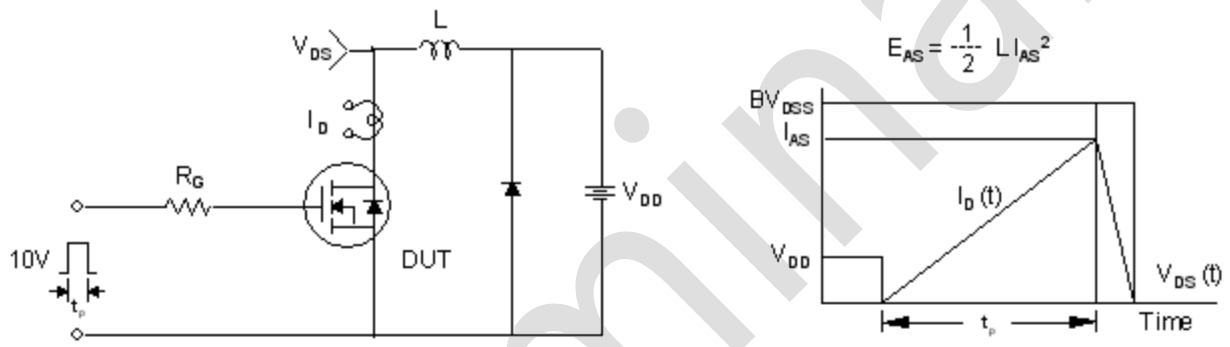

Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

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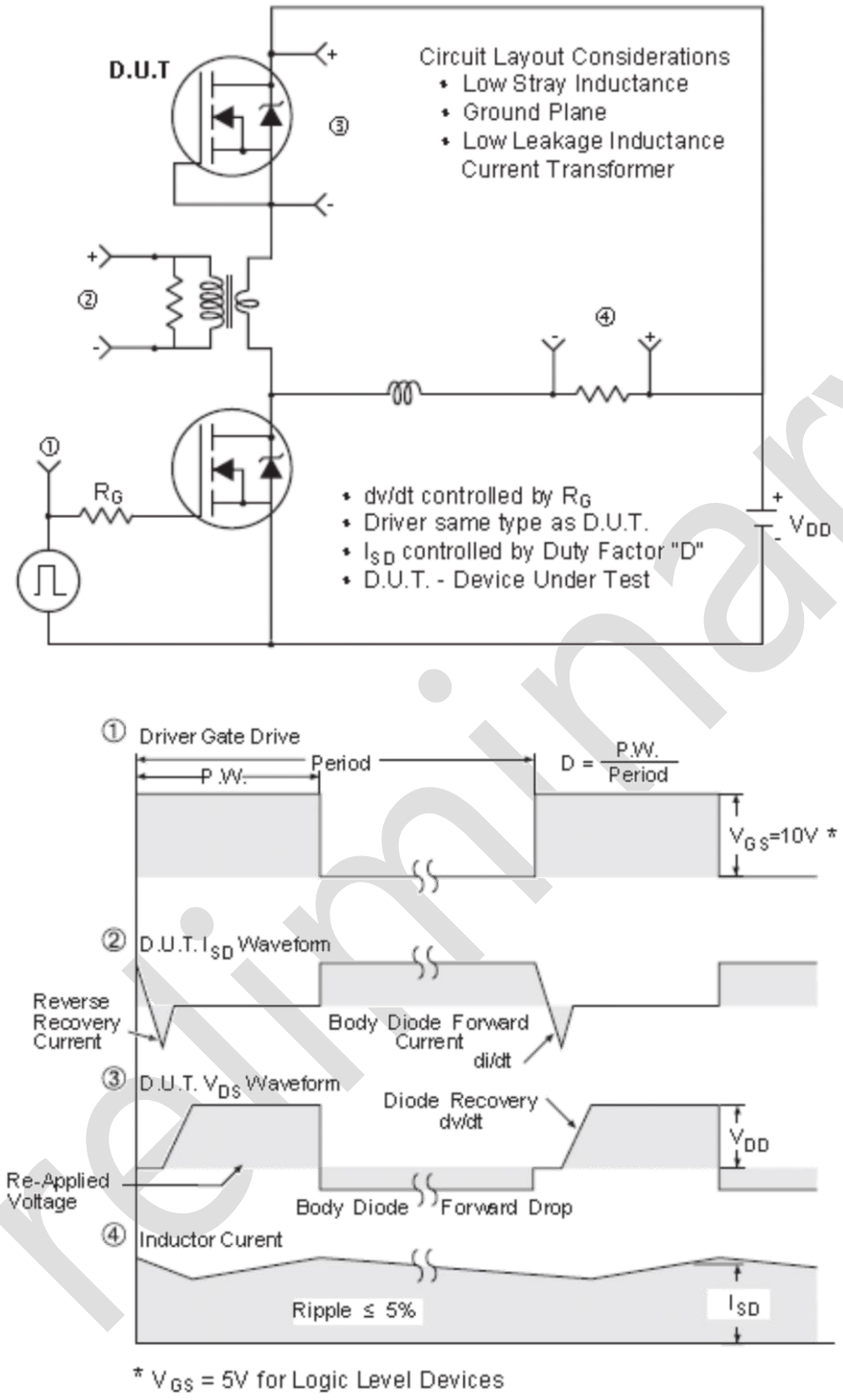

Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

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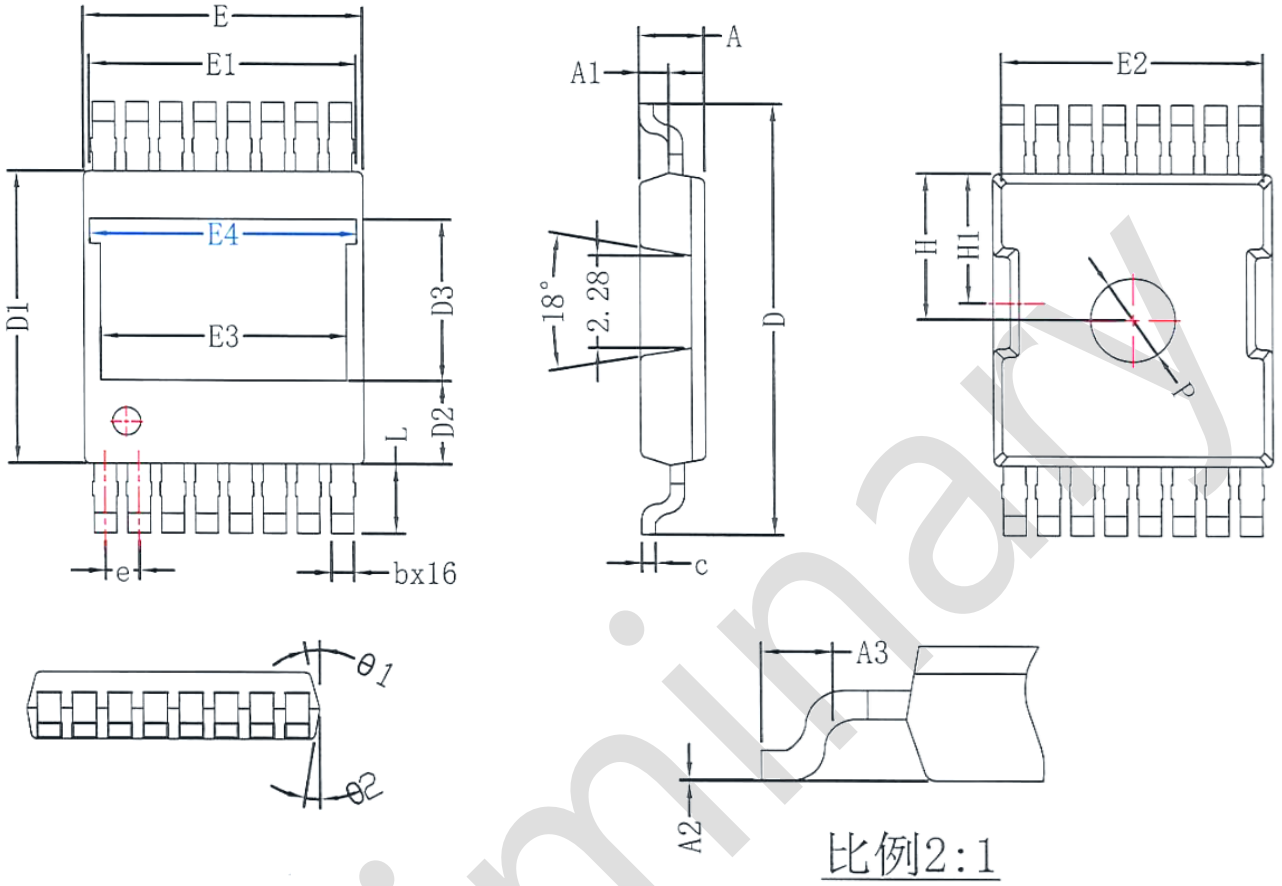
Package outline



SYMBOL	mm		
	MIN	NOM	MAX
※A	2.25	2.30	2.35
※A1	1.00	1.04	1.08
※A2	0.01	0.08	0.16
A3	1.50REF		
※b	0.68	0.70	0.74
※c	0.45	0.50	0.55
※D	14.80	15.00	15.20
※D1	1.00	10.10	10.30
D2	2.60	2.80	3.00
D3	5.77REF		
※E	9.70	9.90	10.10

SYMBOL	mm		
	MIN	NOM	MAX
E1	9.46REF		
E2	9.25REF		
E3	8.25REF		
E4	8.70REF		
※e	1.18	1.20	1.22
※H	5.00	5.20	5.40
H1	4.40	4.60	4.80
※L	2.40	2.45	2.50
※P	2.80	3.00	3.20
θ1	7°	–	9°
θ2	7°	–	9°

Note: ※ Is the key control size.

Figure 19. TOLT Package outline

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