Description

100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

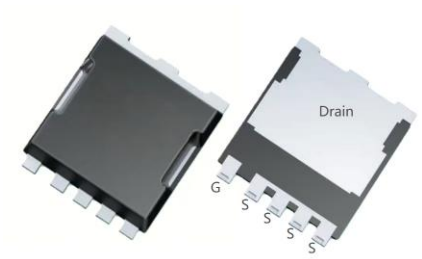
Features

- Device Rating V_{DS} = 100V, I_D = 262A
- $R_{DS(ON)}$ =2.0mΩ (typ.) @ V_{GS} = 10V, I_D = 100A
- Advanced Split Gate Trench Device Design
- RoHS Compliant & Halogen-Free
- Qualified according to JEDEC for target applications
- 100% Avalanche Test

Application

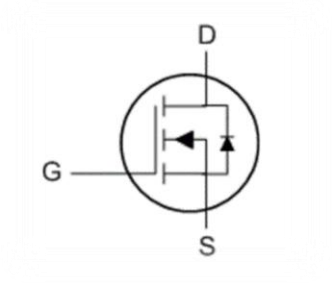
- Brushless DC Motor Control
- DC-DC Converters
- Telecom and Server Power Supply
- High Performance Synchronous Rectification
- Load Switch and eFuse

Package



sTOLL

JFG258N100X



Absolute Maximum Ratings T_J=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		100	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	262	A
		T_C = 100℃	165	A
I_{DM}	Pulsed Drain Current note2		1048	A
P_D	Power Dissipation note4	T_C = 25℃	320	W
	Power Dissipation	T_A = 25℃	3.1	W
E_{AS}	Single Pulsed Avalanche Energy note3		886	mJ
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Thermal characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1	-	0.39	-	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	-	-	40	℃/W

Electrical Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Units
Off Characteristic							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		100	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} =100V, V_{GS}= 0V, T_J = 25℃		-	-	1	μA
		V_{DS} =100V, V_{GS} = 0V, T_J = 125℃		-	-	100	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V		-100	-	100	nA
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		2.2	-	3.8	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =100A		-	2.0	2.4	mΩ
		V_{GS} = 6V, I_D =50A		-	2.8	3.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 1V, I_D =100A		-	180	-	S
Dynamic Characteristics							
R_g	Gate Resistance	f=1MHz		-	0.5	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz		-	4810	-	pF
C_{oss}	Output Capacitance			-	2160	-	pF
C_{rss}	Reverse Transfer Capacitance			-	48	-	pF
Q_g	Total Gate Charge	V_{DS} =50V, I_D = 100A, V_{GS} = 10V		-	76	-	nC
Q_{gs}	Gate-Source Charge			-	21	-	nC
Q_{gd}	Gate-Drain("Miller") Charge			-	20	-	nC
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 100A, R_G = 1Ω, V_{GS} = 10V		-	36	-	ns
t_r	Turn-On Rise Time			-	43	-	ns
$t_{d(off)}$	Turn-Off Delay Time			-	42	-	ns
t_f	Turn-Off Fall Time			-	15	-	ns
Source-Drain Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Diode Forward Current note1,5			-	-	262	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5			-	-	1048	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_F = 100A, V_{GS} = 0V di/dt = 100A/μs		-	71	-	ns
Q_{rr}	Reverse Recovery Charge			-	91	-	nC
V_{SD} note2	Diode Forward Voltage	I_S = 100A, V_{GS} = 0V	T_J = 25°C	-	0.85	-	V
			T_J = 125°C	-	0.75	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.5mH, I_{AS}= 62 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

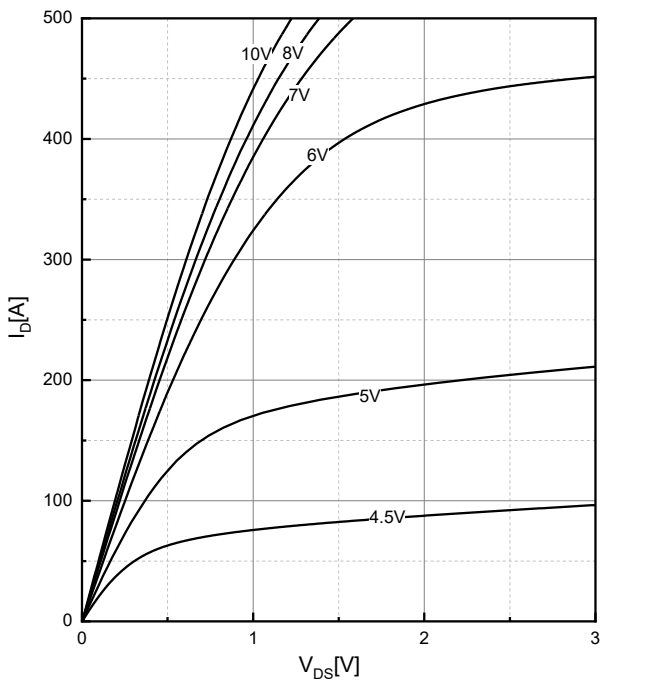


Figure 1. Output Characteristics, T_J=25℃

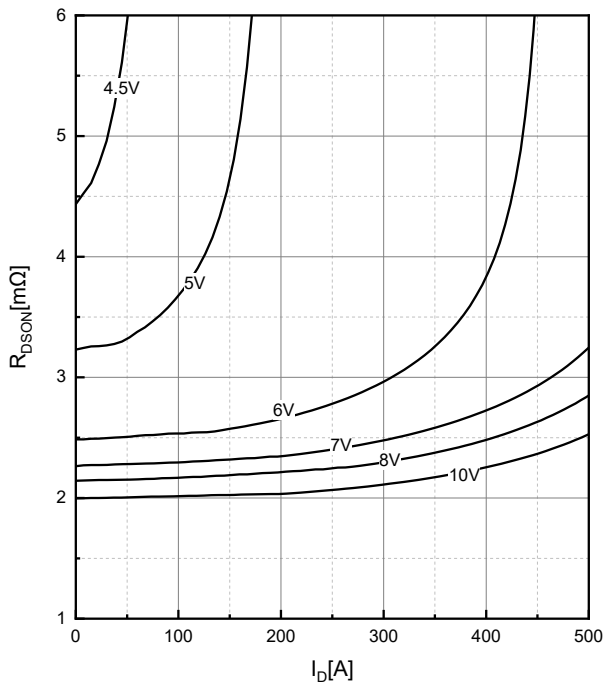


Figure 2. Drain-source on resistance , T_J=25℃

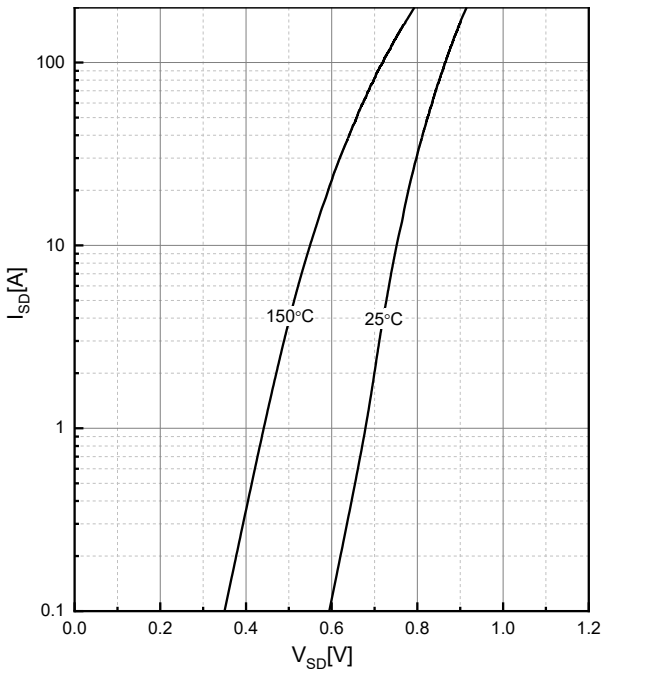


Figure 3. Forward characteristics of body diode

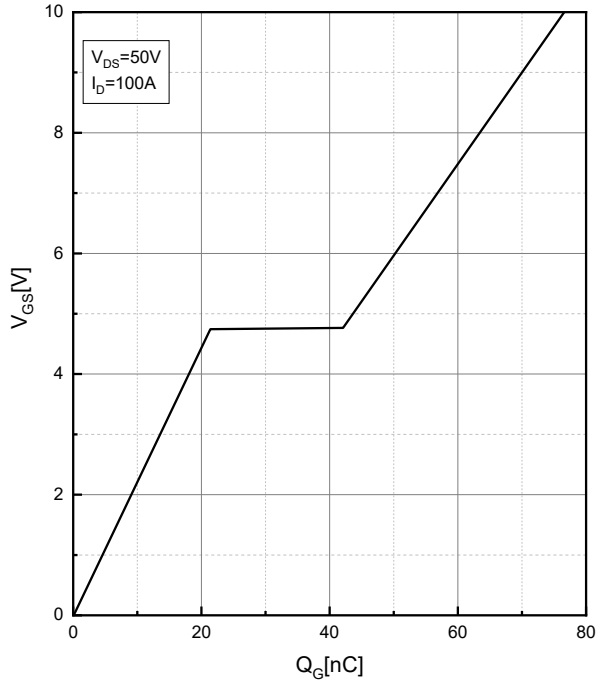


Figure 4. Gate Charge Characteristics

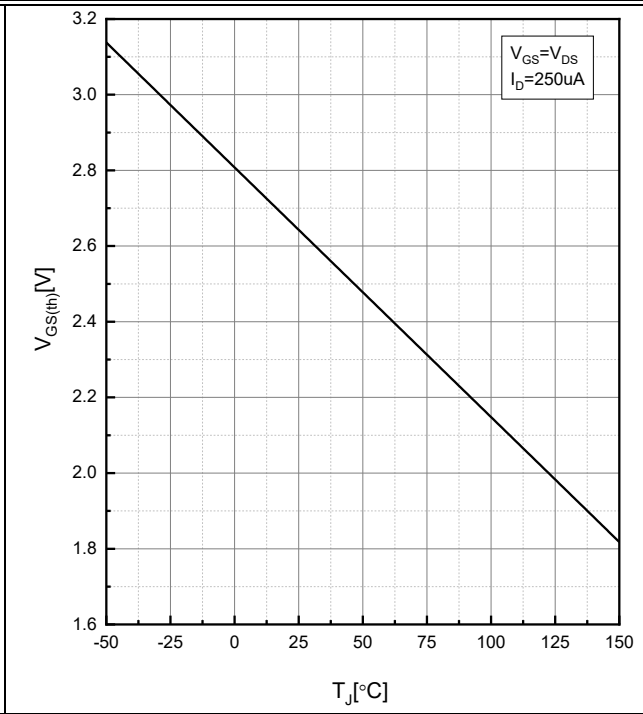


Figure 5. Capacitance Characteristics

Figure 6. Threshold Voltage Vs. Temperature

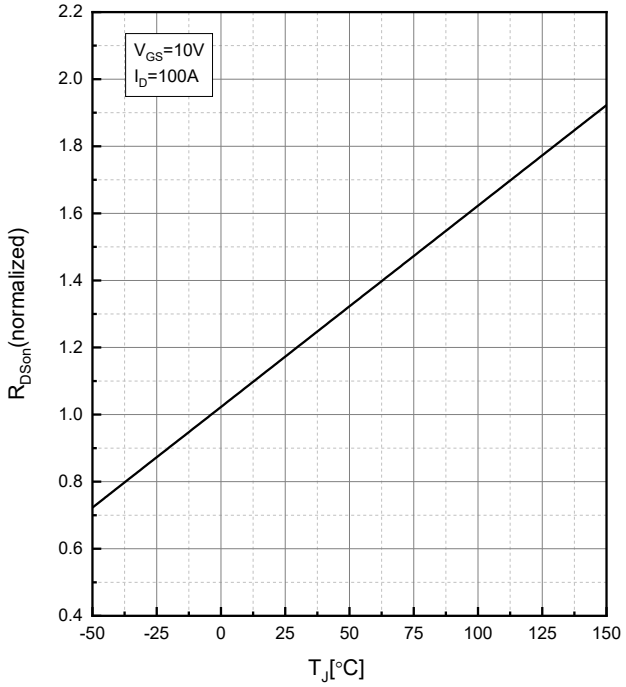


Figure 7. Drain-source on-state resistance

Figure 8. Maximum Safe Operating Area

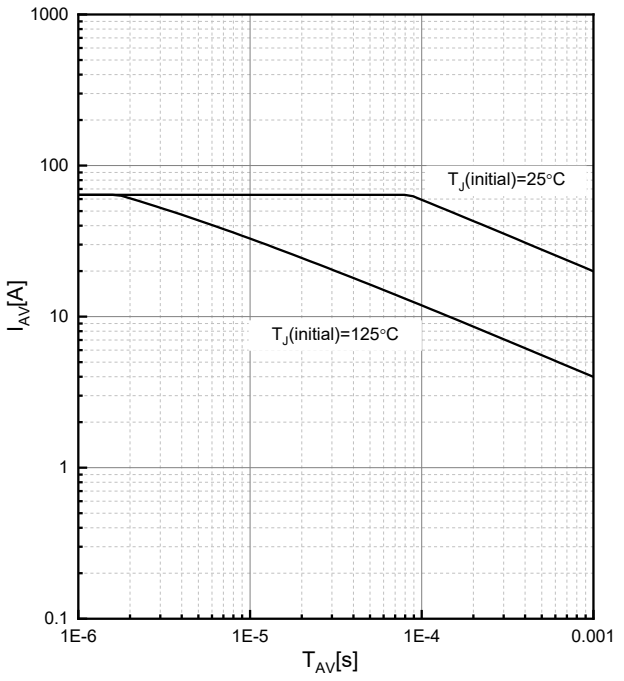


Figure 9. Avalanche characteristics

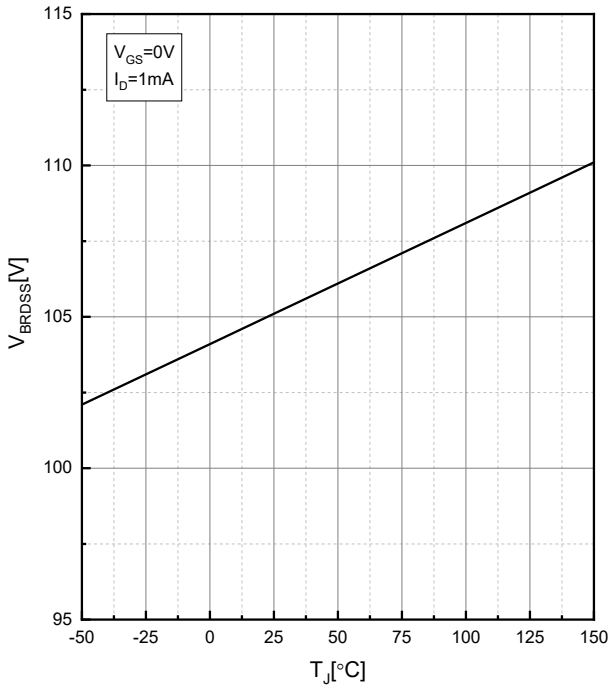


Figure 10. Drain-source breakdown voltage

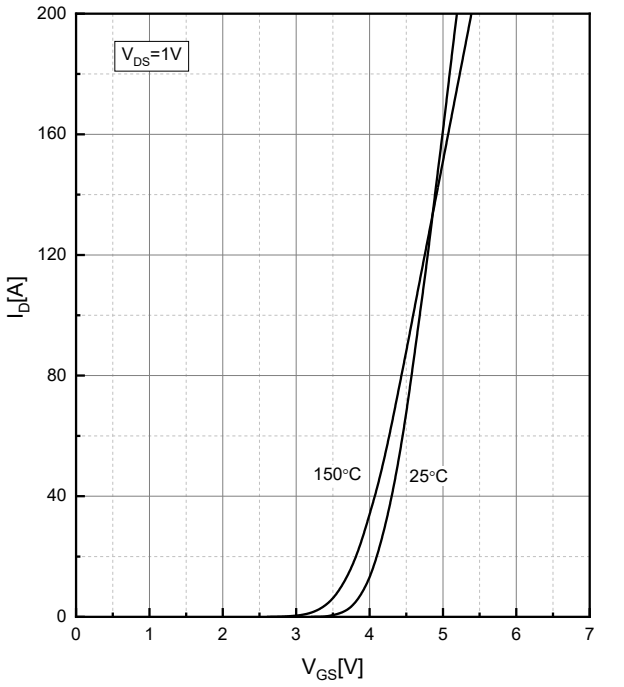


Figure 11. Transfer characteristics

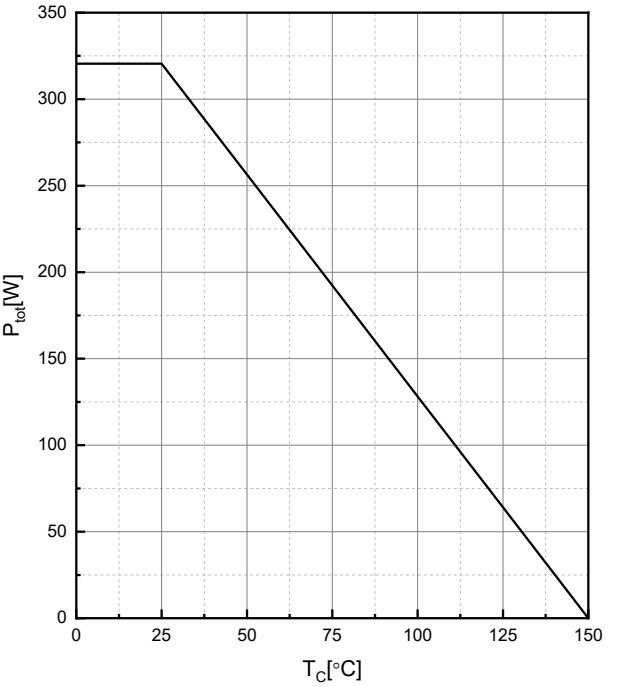


Figure 12. Power dissipation

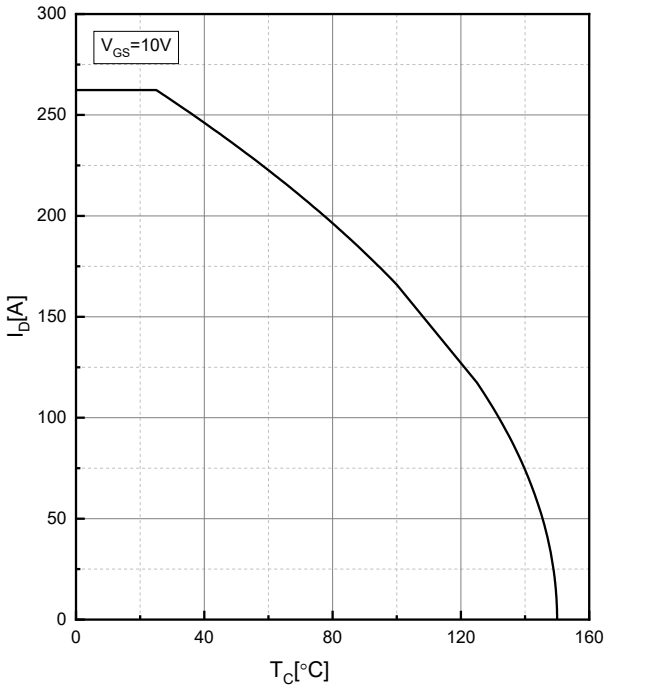


Figure 13. Drain current

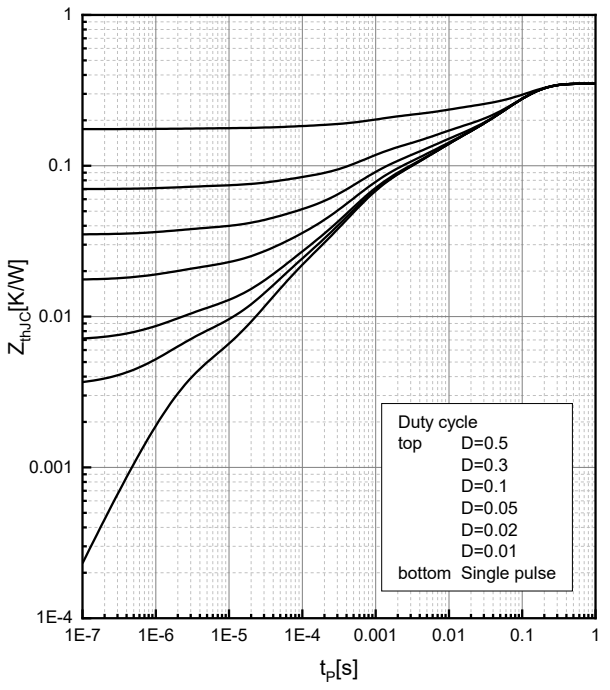


Figure 14. Effective Transient Thermal Impedance

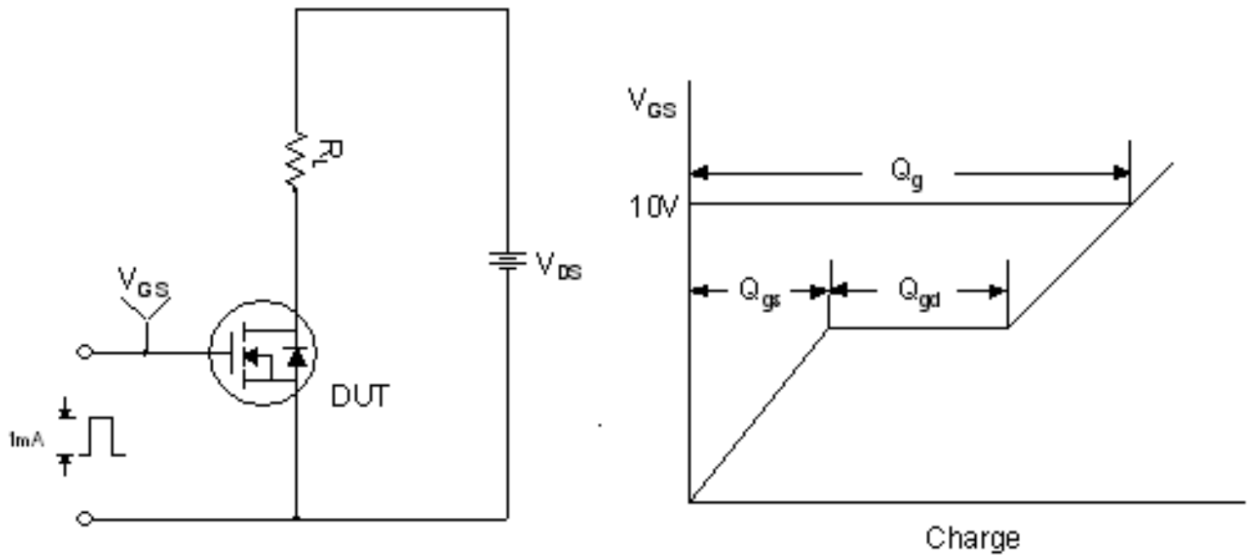


Figure 15. Gate Charge Test Circuit & Waveform

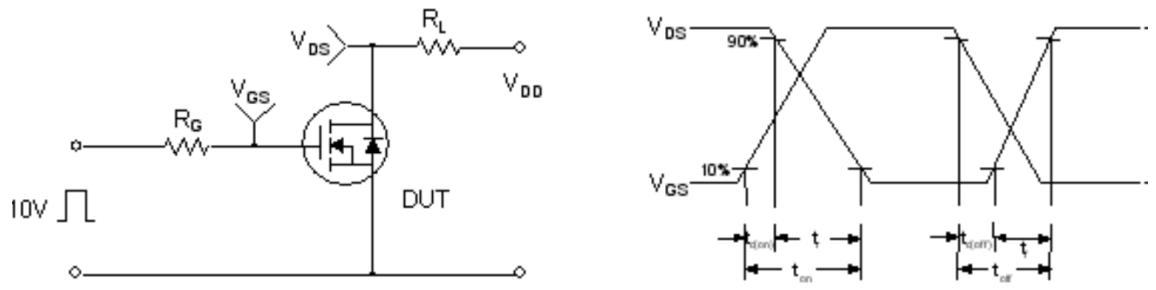


Figure 16. Resistive Switching Test Circuit & Waveforms

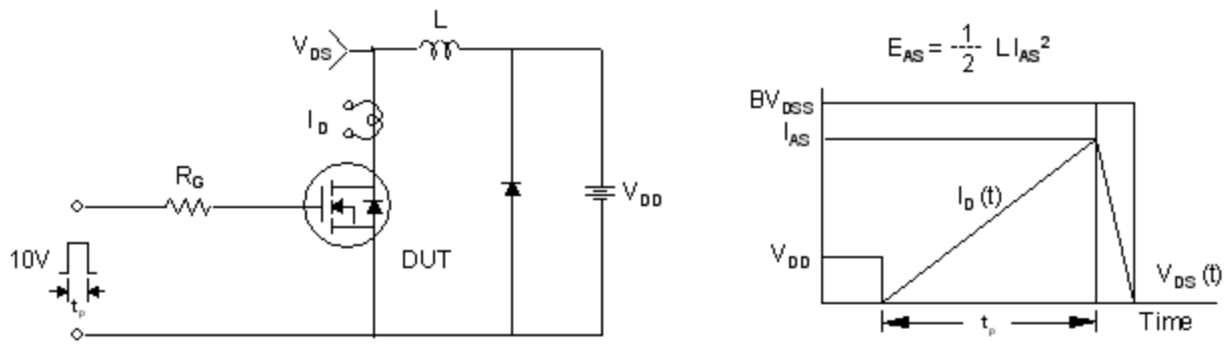


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

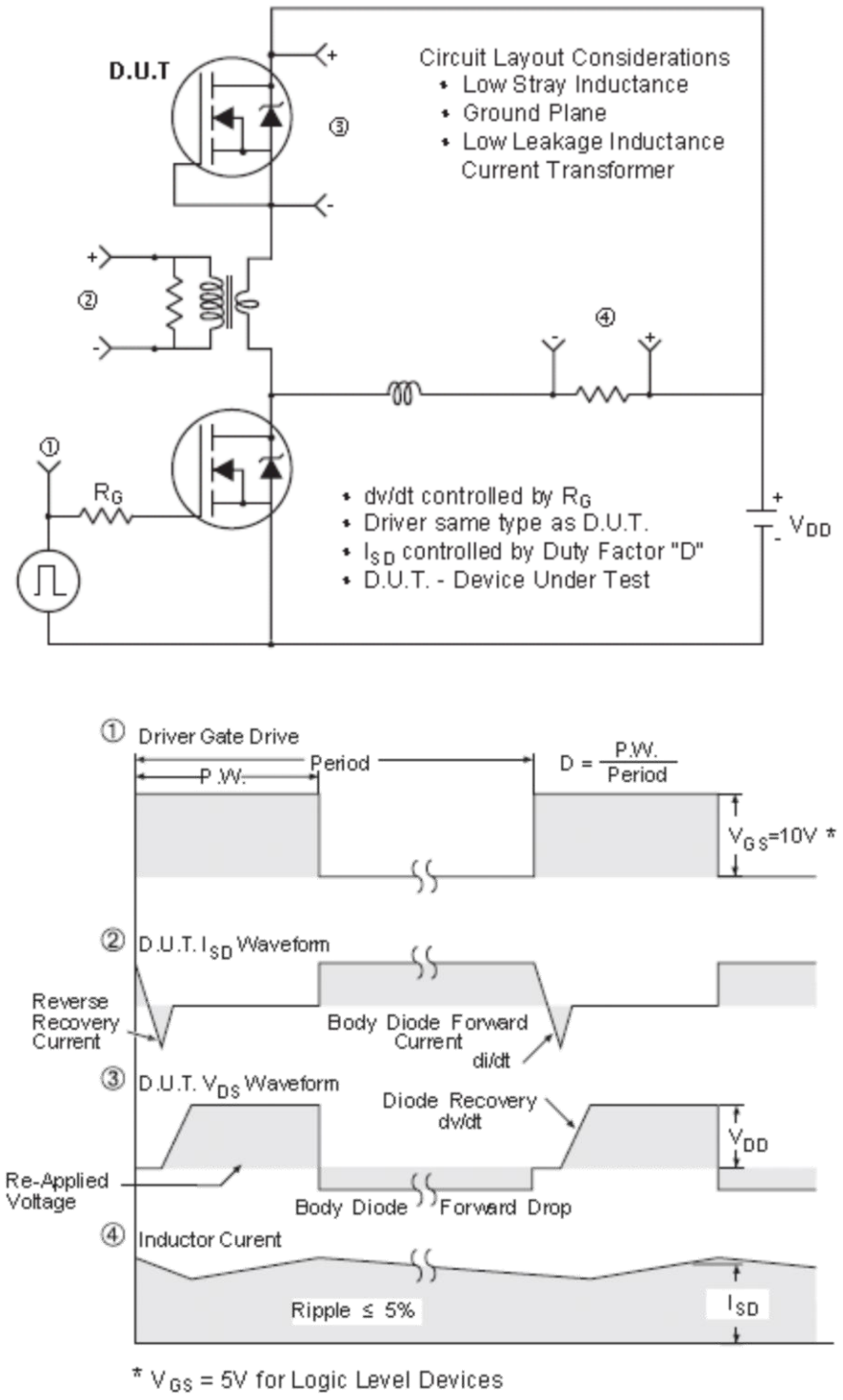
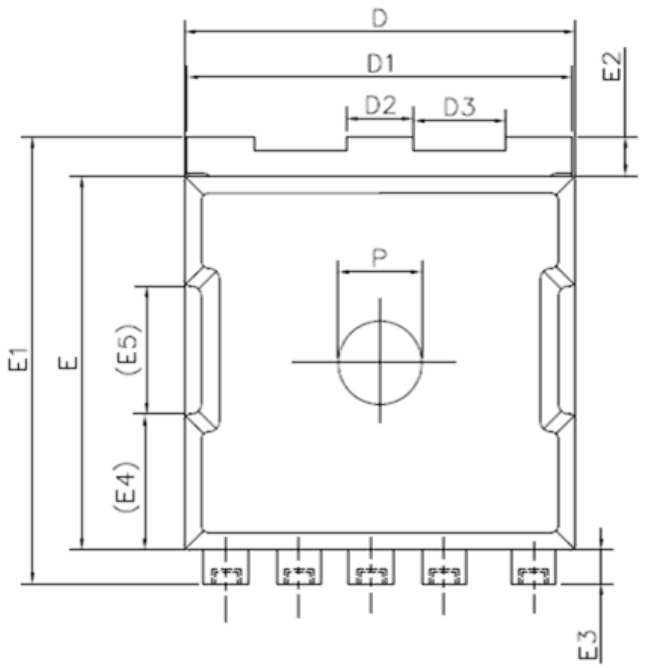
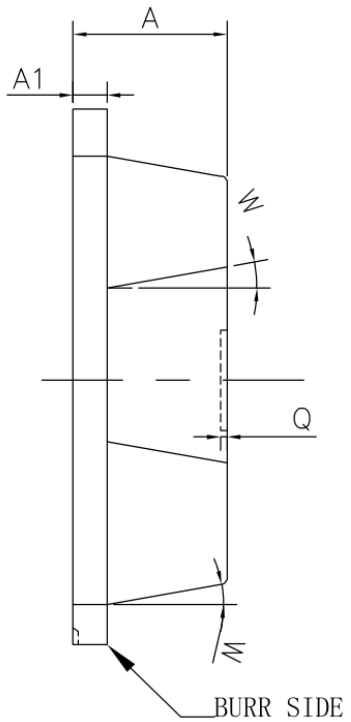
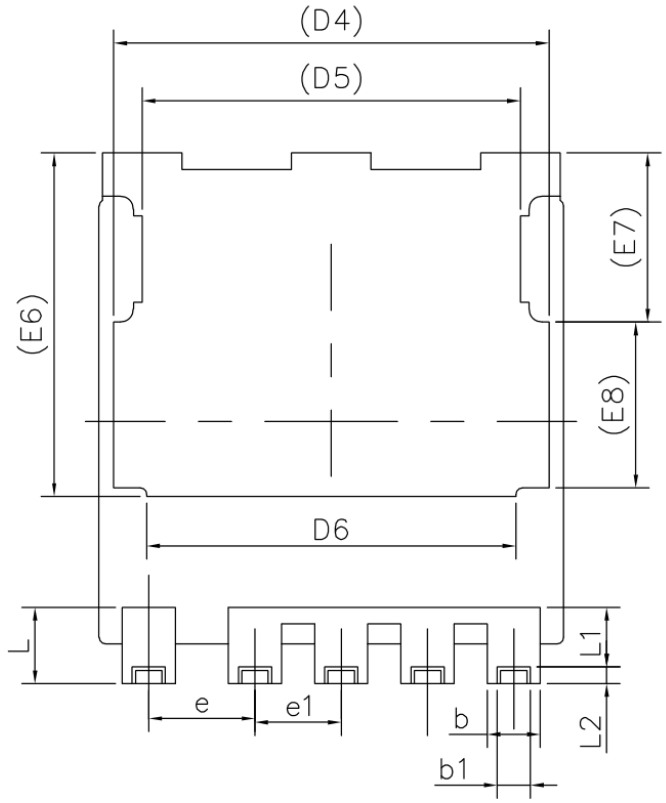


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline







DIMENSION	MILLIMETERS		
	MIN	A	MAX
A	2.20	2.30	2.40
A1	0.40	0.50	0.60
b	0.70	0.80	0.90
b1	0.40	0.50	0.60
D	6.80	7.0	7.20
D1	6.80	6.9	7.20
D2	1.10	1.20	1.30
D3	1.55	1.65	1.75
D4	6.56		
D5	5.70		
D6	5.56		
E	6.50	6.70	6.9
E1	7.80	8.0	8.2
E2	0.60	0.7	0.80
E3	0.50	0.60	0.70
E4	2.43		
E5	2.30		
E6	5.18		
E7	2.55		
E8	2.50		
e	1.60		
e1	1.30		
L	1.05	1.15	1.25
L1	0.80	0.90	1.0
L2	0.15	0.25	0.35
P	1.40	1.50	1.60
Q	0	0.08	0.10
W	8°	10°	11°

Figure 19. sTOLL Package outline

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