Description

150V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

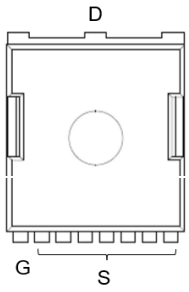
Features

- Device Rating V_{DS} = 150V, I_D = 205A
- $R_{DS(ON)}$ = 2.8mΩ (typ.) @ V_{GS} = 10V, I_D = 50A
- Advanced Split Gate Device Design
- RoHS Compliant & Halogen-Free
- Qualified according to JEDEC for target applications
- 100% avalanche test

Application

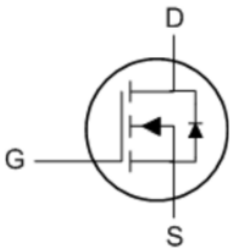
- High Performance Synchronous Rectification
- Brushless DC Motor Control
- Load Switch and eFuse
- Battery Protection

Package



TOLL

JFG205N150Q



Absolute Maximum Ratings T_J=25℃ unless otherwise specified

Symbol	Parameter		Value	Units
V_{DS}	Drain-Source Voltage		150	V
V_{GS}	Gate-Source Voltage		± 20	V
I_D	Continuous Drain Current, VGS @ 10V note1	T_C = 25℃	205	A
		T_C = 100℃	130	A
I_{DM}	Pulsed Drain Current note2		820	A
P_D	Power Dissipation note4	T_C = 25℃	312	W
	Power Dissipation	T_A = 25℃	3.12	W
E_{AS}	Single Pulsed Avalanche Energy note3		1693	mJ
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Thermal characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case note1	-	0.4	-	℃/W
$R_{\theta JA}$	Junction-to-Ambient (mounted on 1 inch square PCB)	-	-	40	℃/W

Electrical Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Units
Off Characteristic							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA		150	-	-	V
I_{DSS}	Drain-Source Leakage Current	V_{DS} = 150V, V_{GS} = 0V,T_J =25℃		-	-	1	μA
		V_{DS} = 150V, V_{GS} = 0V, T_J =125℃		-	-	100	μA
I_{GSS}	Gate-Source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V		-100	-	100	nA
On Characteristics							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA		3.0	-	4.6	V
$R_{DS(on)}$	Static Drain-Source On-Resistance note2	V_{GS} = 10V, I_D =50A		-	2.8	3.4	mΩ
		V_{GS} = 8V, I_D =25A		-	3.0	3.6	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 1V, I_D =50A		-	150	-	S
Dynamic Characteristics							
R_g	Gate Resistance	f=1.0MHz		-	0.5	-	Ω
C_{iss}	Input Capacitance	V_{DS} = 75V, V_{GS} = 0V, f = 1.0MHz		-	9700	-	pF
C_{oss}	Output Capacitance			-	830	-	pF
C_{rss}	Reverse Transfer Capacitance			-	14	-	pF
Q_g	Total Gate Charge	V_{DS} =75V, I_D = 50A, V_{GS} = 10V		-	137	-	nC
Q_{gs}	Gate-Source Charge			-	50	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge			-	28	-	nC
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 75V, I_D = 50A, R_G = 1Ω, V_{GS} = 10V		-	26	-	ns
t_r	Turn-On Rise Time			-	28	-	ns
$t_{d(off)}$	Turn-Off Delay Time			-	44	-	ns
t_f	Turn-Off Fall Time			-	16	-	ns
Source-Drain Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Diode Forward Current note1,5			-	-	205	A
I_{SM}	Maximum Pulsed Diode Forward Current note2,5			-	-	820	A
t_{rr}	Reverse Recovery Time	T_J = 25°C, I_S = 50A, V_{GS} = 0V , di/dt = 400A/μs		-	56	-	ns
Q_{rr}	Reverse Recovery Charge			-	128	-	nC
V_{SD} note2	Diode Forward Voltage	I_S = 20A, V_{GS} = 0V	T_J = 25°C	-	0.80	-	V
			T_J = 125°C	-	0.68	-	V

Note :

1.The data tested by surface mounted on one $inch^2$ FR-4 board with 2OZ copper.

2.The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.

3.The EAS data shows Max. rating. The test condition is L=0.5mH, I_{AS}= 86 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Performance Characteristics

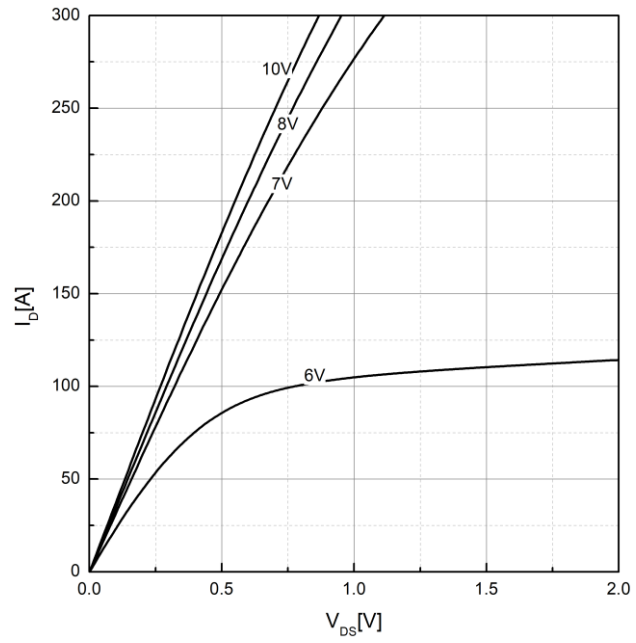


Figure 1. Output Characteristics, T_J=25℃

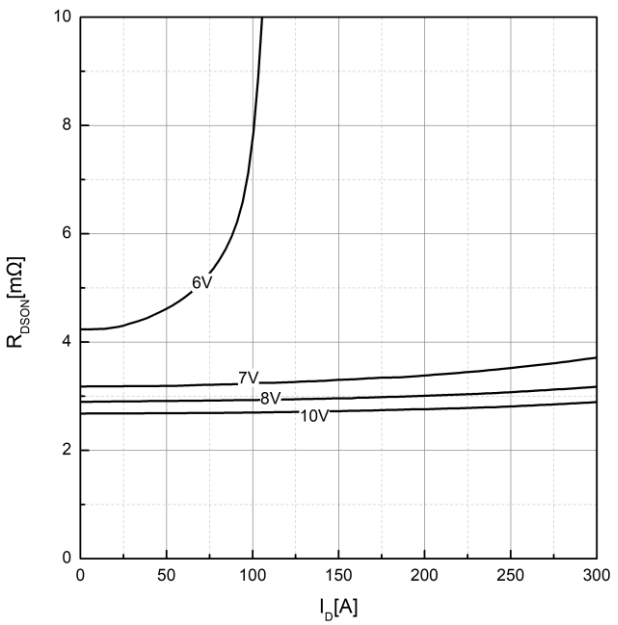


Figure 2. Drain-source on resistance , T_J=25℃

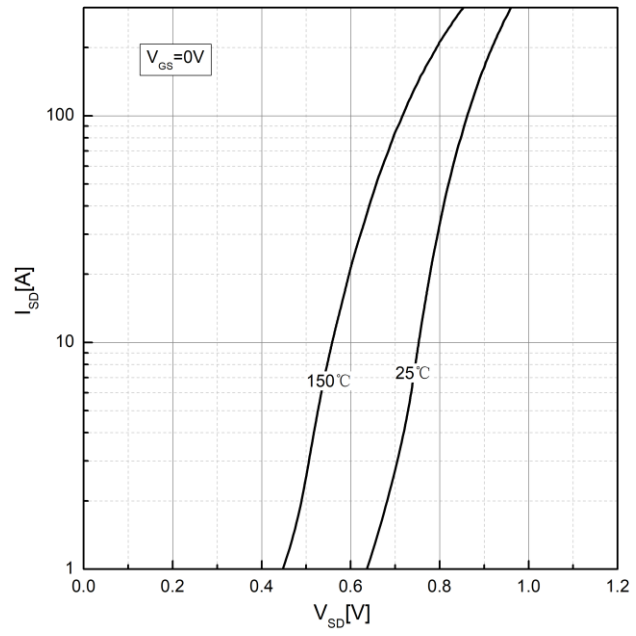


Figure 3. Forward characteristics of body diode

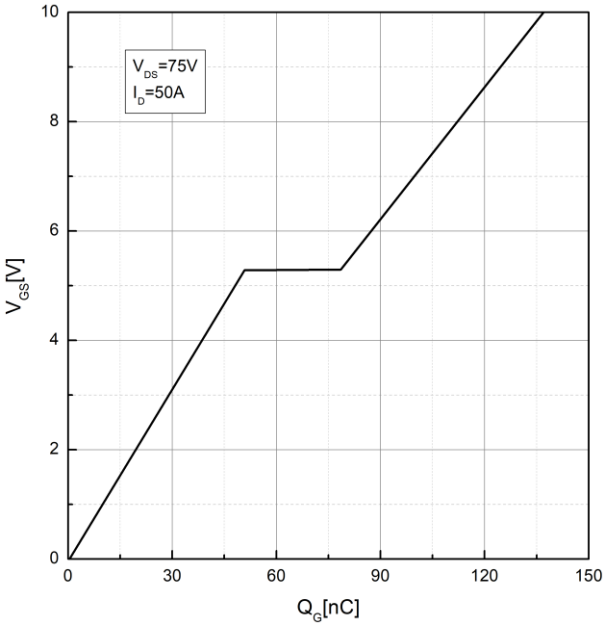


Figure 4. Gate Charge Characteristics

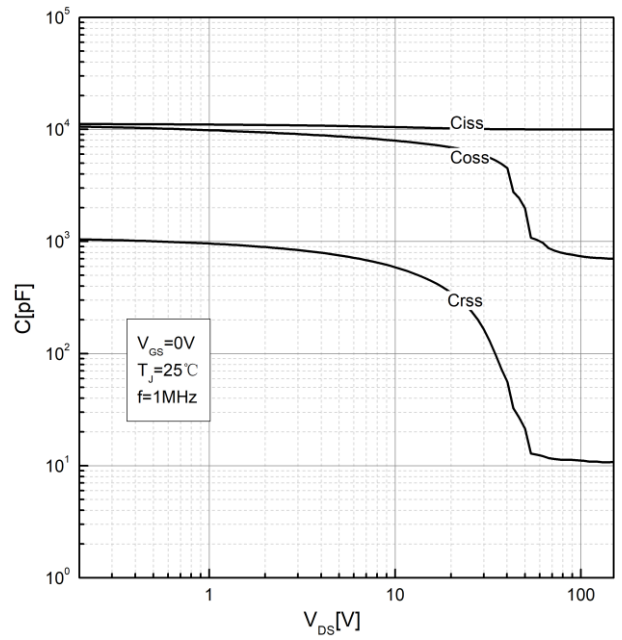


Figure 5. Capacitance Characteristics

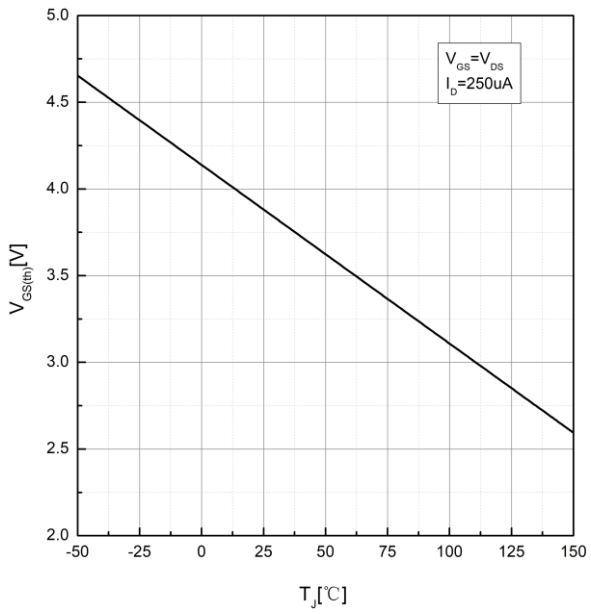


Figure 6. Threshold Voltage Vs. Temperature

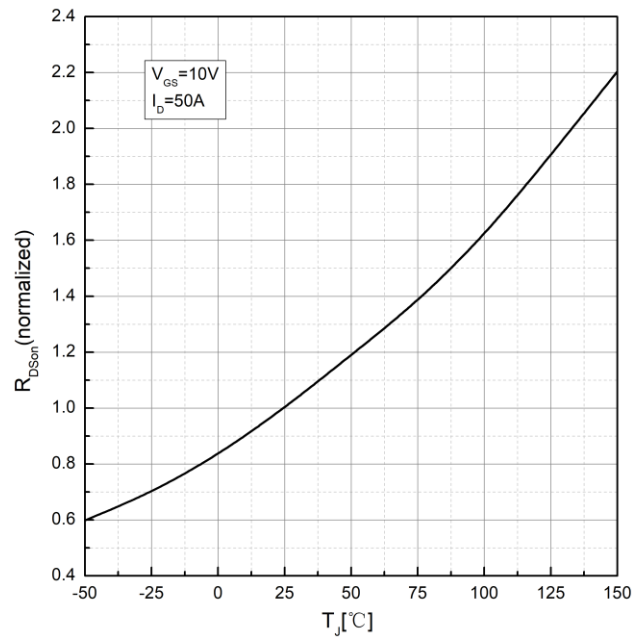


Figure 7. Drain-source on-state resistance

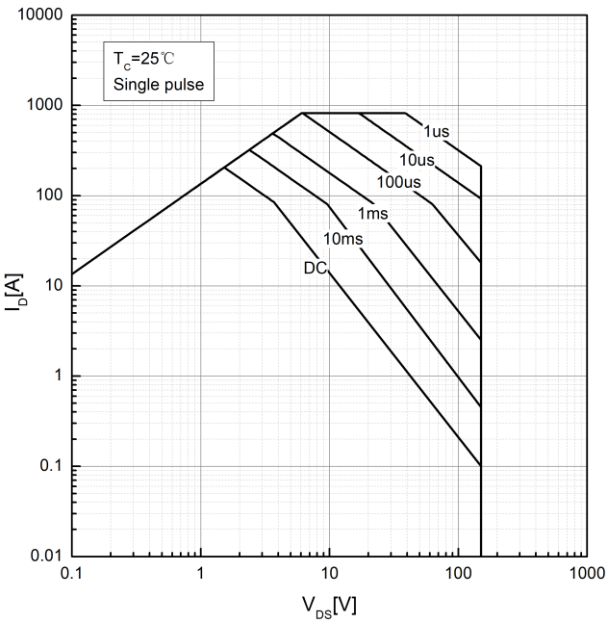


Figure 8. Maximum Safe Operating Area

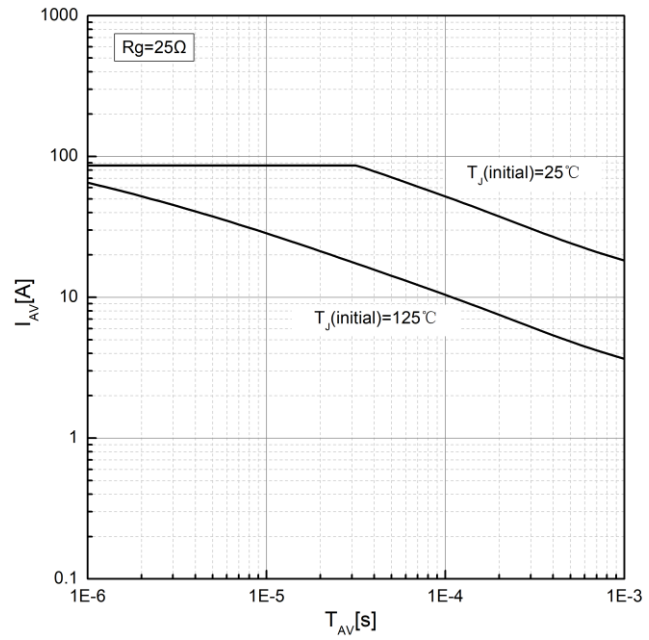


Figure 9. Avalanche characteristics

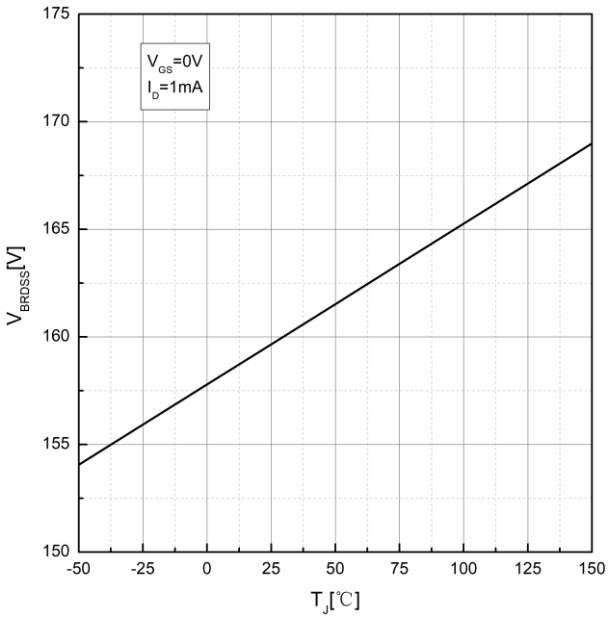


Figure 10. Drain-source breakdown voltage

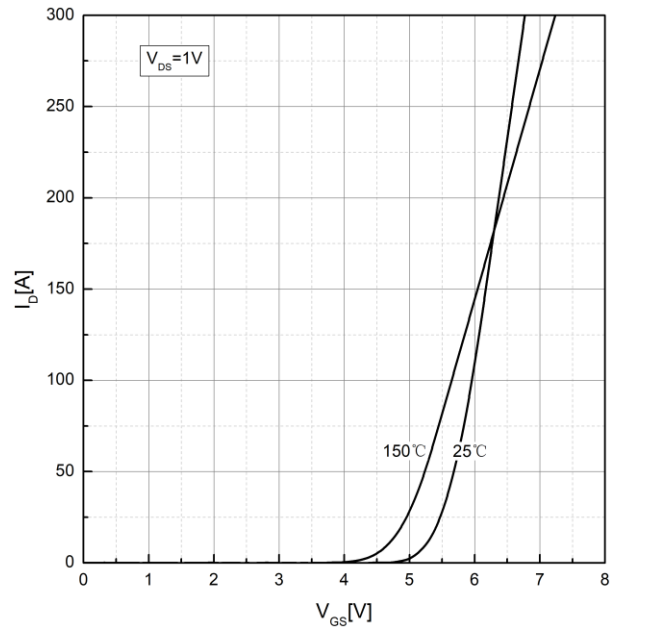


Figure 11. Transfer characteristics

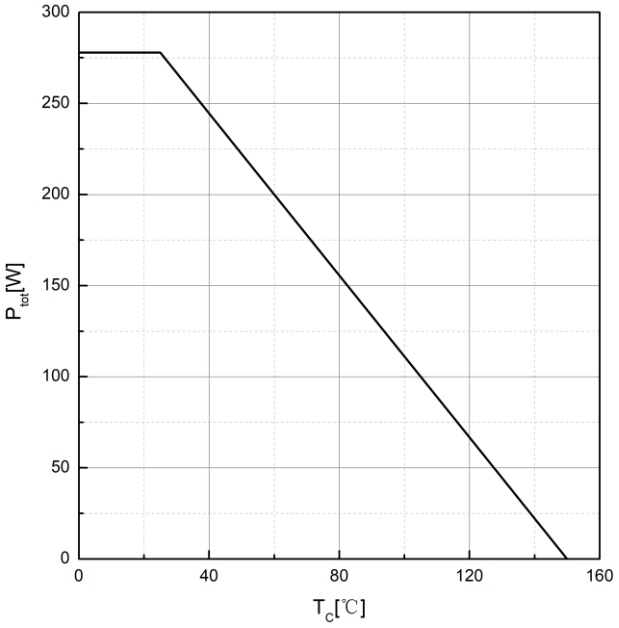


Figure 12. Power dissipation

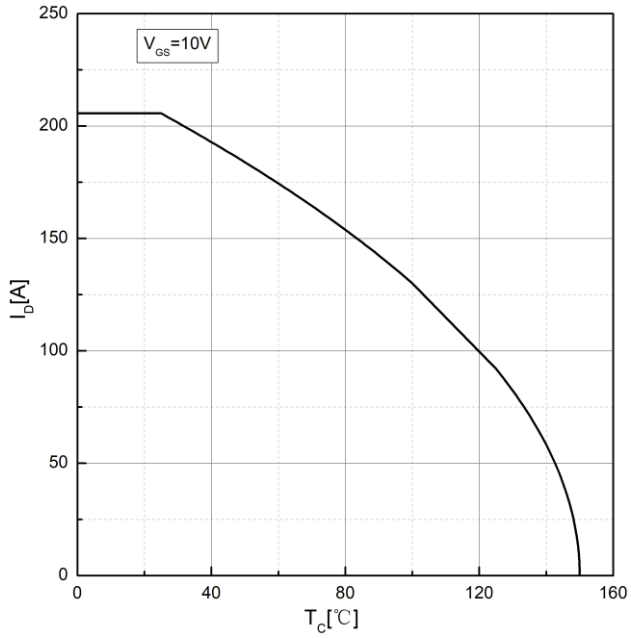


Figure 13. Drain current

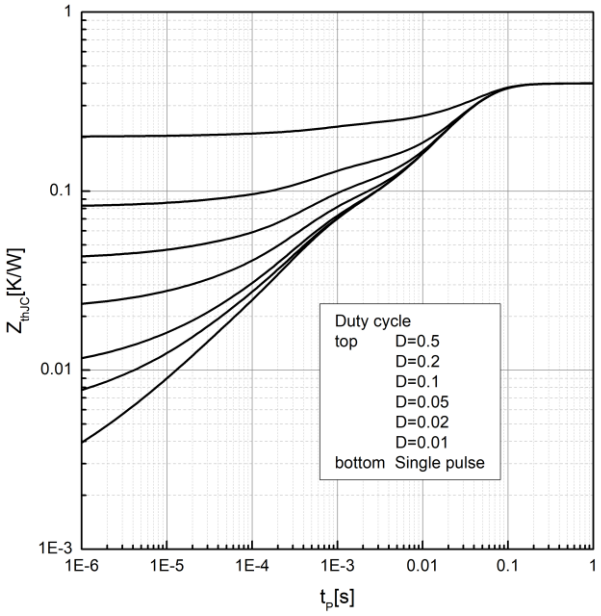


Figure 14. Effective Transient Thermal Impedance

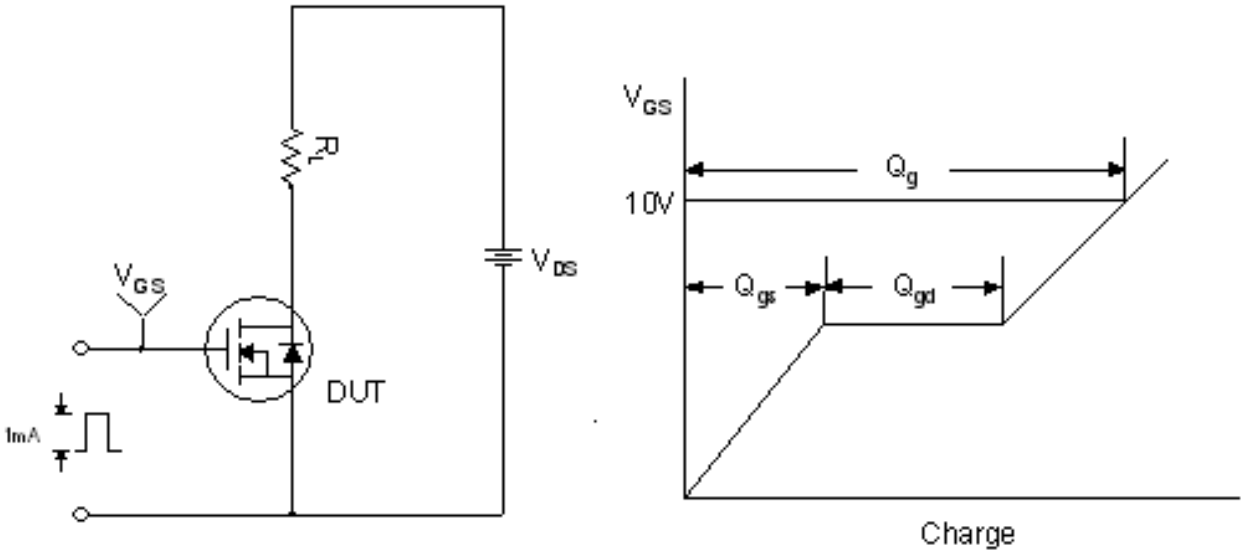


Figure 15. Gate Charge Test Circuit & Waveform

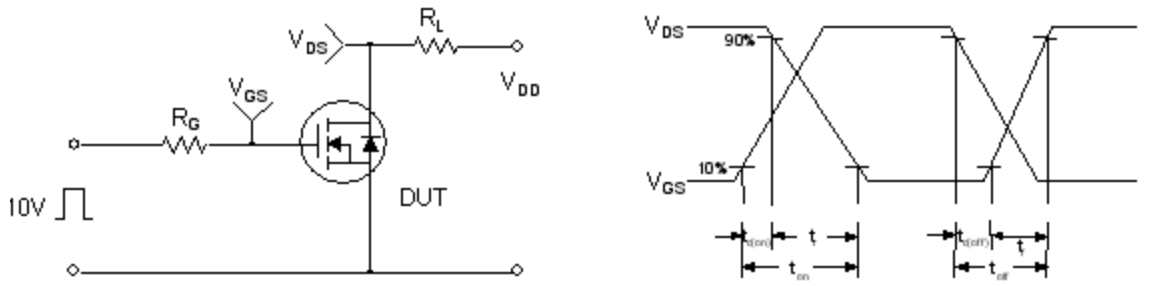


Figure 16. Resistive Switching Test Circuit & Waveforms

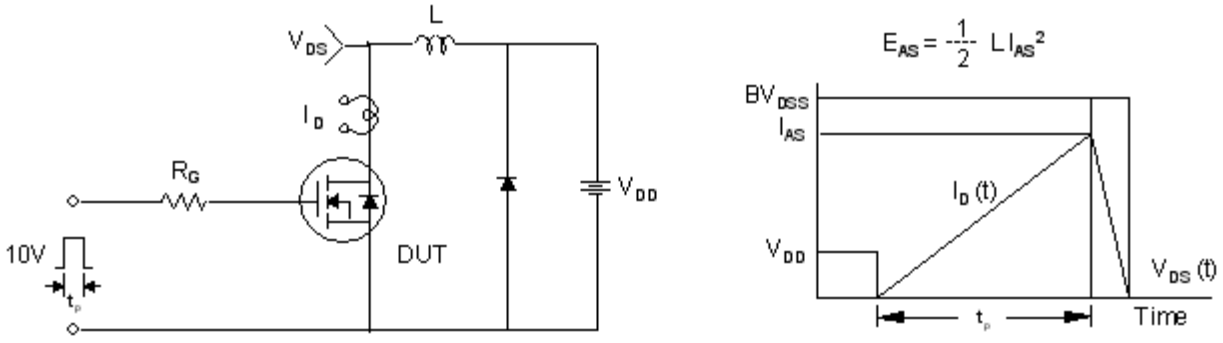


Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms

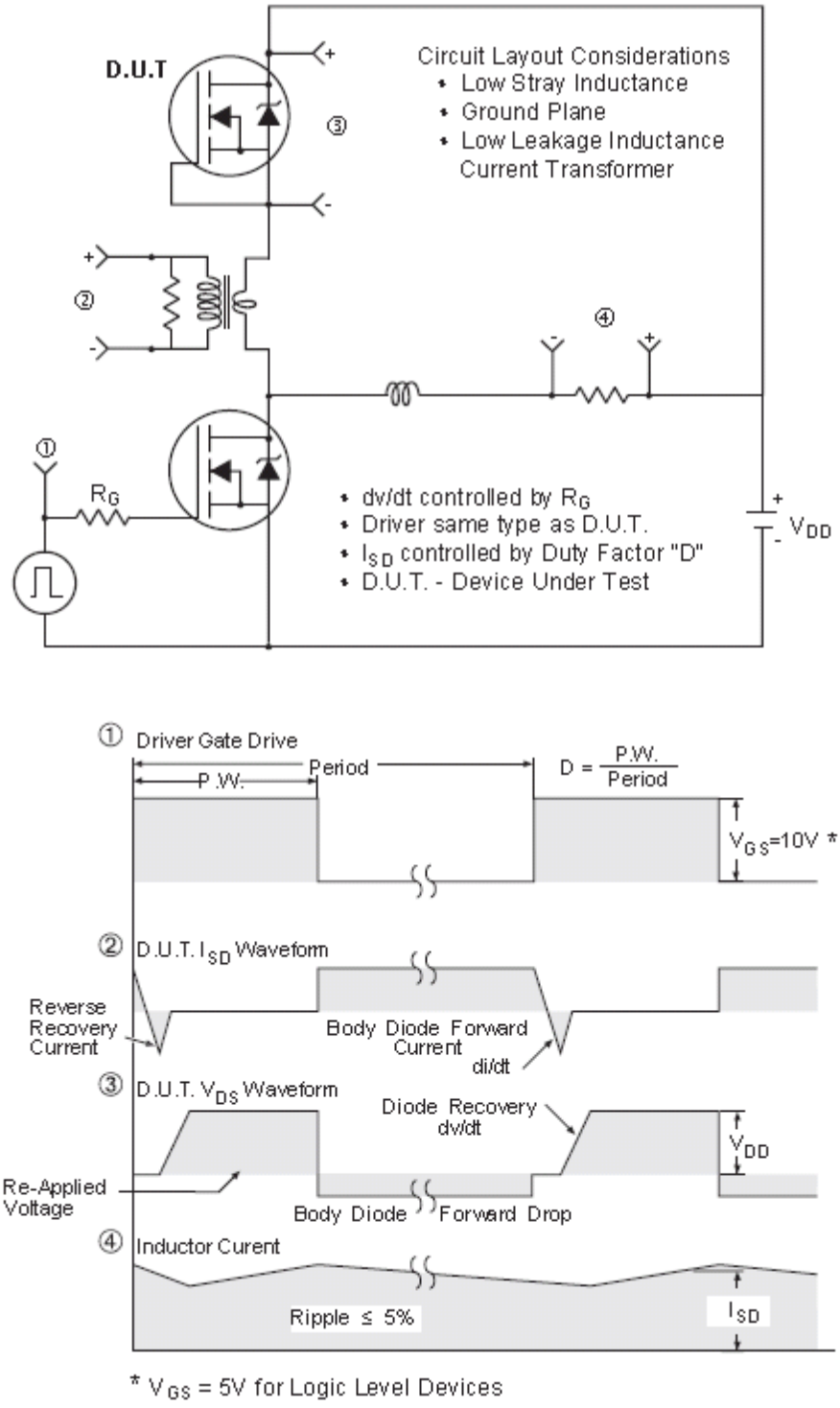
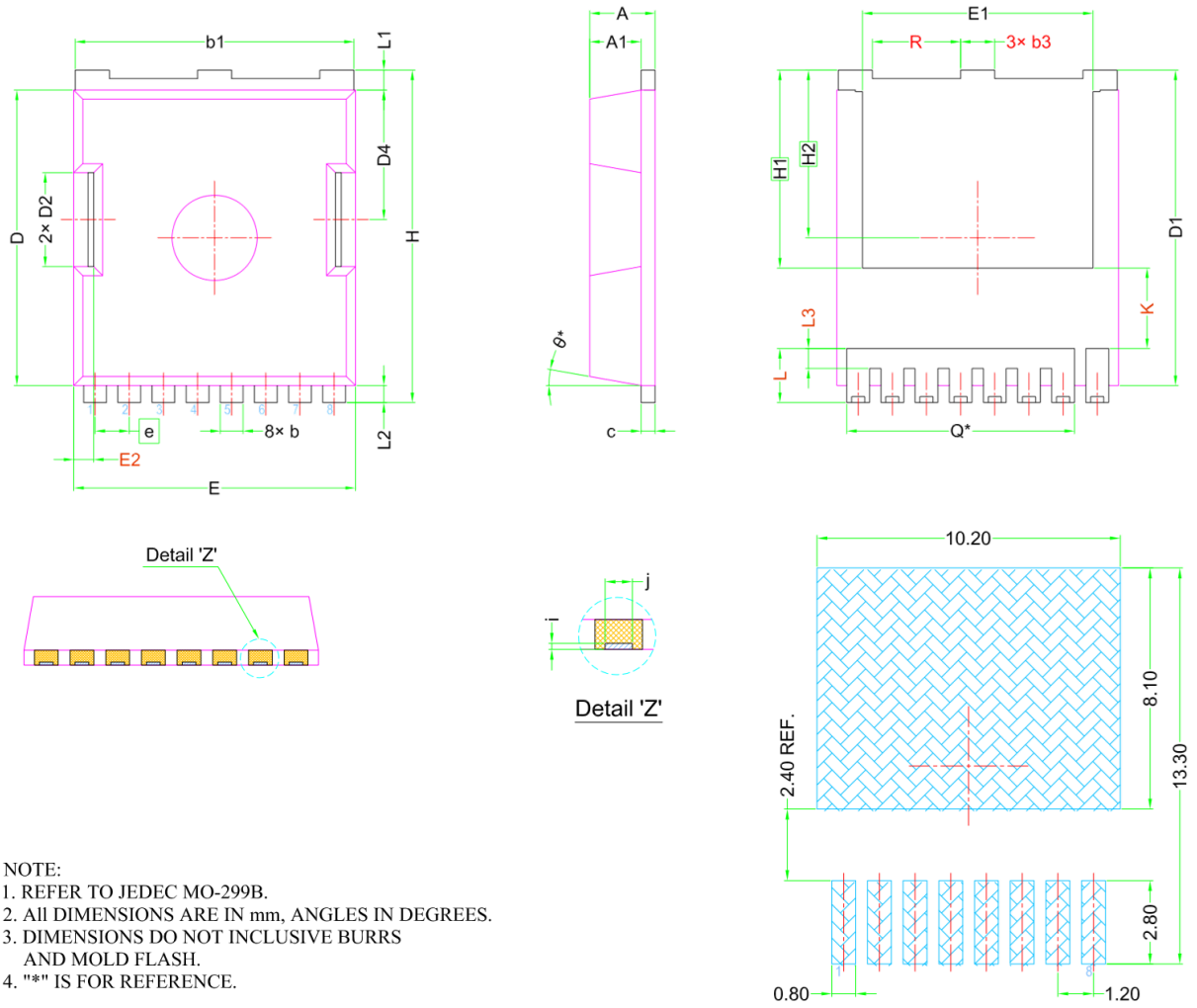


Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package outline



NOTE:
1. REFER TO JEDEC MO-299B.
2. All DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
3. DIMENSIONS DO NOT INCLUSIVE BURRS AND MOLD FLASH.
4. "*" IS FOR REFERENCE.

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	1 0.00
E1	8.00	8.10	8.20
E2	0.60	0.70	0.80
e	1.20 BSC		

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
N	8		
Q	8.00 REF.		
R	3.00	3.10	3.20
θ	10° REF.		

Figure 19. TOLL Package outline

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